UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,116	08/29/2001	William R. Wheeler	10559/601001/P12885	6930

20985 7590 01/14/2005		EXAMINER
FISH & RICHARDSON, PC		FERRIS III, FRED O
12390 EL CAMINO REAL		
SAN DIEGO, CA 92130-2081	ART UNIT	PAPER NUMBER
	2128	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/942,116	WHEELER ET AL.
	Examiner	**Art Unit**	
	Fred Ferris	2128	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>29 August 2001</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-24</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-24</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>11 June 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>12/29, 6/11/03, 8/29</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-24 have been presented for examination based on applicant's

disclosure filed on 29 August 2001. Claims 1-24 have been rejected by the examiner.

Specification

2.   The disclosure is also objected to because the Summary of the Invention section

is missing from the disclosure. Applicants are reminded of proper content of the

specification. See MPEP § 608.01(d)

Content of Specification

(a)   <u>Title of the Invention</u>: See 37 CFR 1.72(a) and MPEP § 606. The title of
        the invention should be placed at the top of the first page of the
        specification unless the title is provided in an application data sheet. The
        title of the invention should be brief but technically accurate and
        descriptive, preferably from two to seven words may not contain more
        than 500 characters.

(b)   <u>Cross-References to Related Applications</u>: See 37 CFR 1.78 and MPEP
        § 201.11.

(c)   <u>Statement Regarding Federally Sponsored Research and Development</u>:
        See MPEP § 310.

(d)   <u>Incorporation-By-Reference Of Material Submitted On a Compact Disc</u>:
        The specification is required to include an incorporation-by-reference of
        electronic documents that are to become part of the permanent United
        States Patent and Trademark Office records in the file of a patent
        application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer
        program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)),
        and tables having more than 50 pages of text were permitted as electronic
        documents on compact discs beginning on September 8, 2000.

Or alternatively, <u>Reference to a "Microfiche Appendix"</u>: See MPEP §
608.05(a). "Microfiche Appendices" were accepted by the Office until
March 1, 2001.

(e)   <u>Background of the Invention</u>: See MPEP § 608.01(c). The specification
       should set forth the Background of the Invention in two parts:

       (1)   <u>Field of the Invention</u>: A statement of the field of art to which the
              invention pertains. This statement may include a paraphrasing of
              the applicable U.S. patent classification definitions of the subject
              matter of the claimed invention. This item may also be titled
              "Technical Field."

       (2)   <u>Description of the Related Art including information disclosed under
              37 CFR 1.97 and 37 CFR 1.98</u>: A description of the related art
              known to the applicant and including, if applicable, references to
              specific related art and problems involved in the prior art which are
              solved by the applicant's invention. This item may also be titled
              "Background Art."

<u>The following section has been omitted from applicant's specification</u>:

(f)   **<u>Brief Summary of the Invention</u>: See MPEP § 608.01(d). A brief
       summary or general statement of the invention as set forth in 37
       CFR 1.73. The summary is separate and distinct from the abstract
       and is directed toward the invention rather than the disclosure as a
       whole. The summary may point out the advantages of the invention
       or how it solves problems previously existent in the prior art (and
       preferably indicated in the Background of the Invention). In chemical
       cases it should point out in general terms the utility of the invention.
       If possible, the nature and gist of the invention or the inventive
       concept should be set forth. Objects of the invention should be
       treated briefly and only to the extent that they contribute to an
       understanding of the invention.**

(g)   <u>Brief Description of the Several Views of the Drawing(s)</u>: See MPEP §
       608.01(f). A reference to and brief description of the drawing(s) as set
       forth in 37 CFR 1.74.

(h)   <u>Detailed Description of the Invention</u>: See MPEP § 608.01(g). A
       description of the preferred embodiment(s) of the invention as required in
       37 CFR 1.71. The description should be as short and specific as is
       necessary to describe the invention adequately and accurately. Where
       elements or groups of elements, compounds, and processes, which are

conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i)   Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j)   Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

Drawings

3.   *Applicant's drawings submitted 11 June 2003 have been approved by the examiner.*

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.   Claims 1-21 are rejected under 35 U.S.C. 112, s cond paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention.

Specifically, independent claims 1, 6, and 11 recite storing a first state of a logic

design weather "a node" has a logic high value, and subsequently storing a second

state of a logic design weather "the node" has a logic low value. In this case it is unclear

if the claim limitations for "a node" and "the node" are referring to the same node, or

simply any node in the simulation. MPEP 2171 requires the following:

*2171   Two Separate Requirements for Claims Under 35 U.S.C. 112, Second
Paragraph*
The second paragraph of 35 U.S.C. 112 is directed to requirements for the claims:

*The specification shall conclude with one or more claims particularly pointing out and
distinctly claiming the subject matter which the applicant regards as his invention.*

There are two separate requirements set forth in this paragraph:
*(A)   the claims must set forth the subject matter that applicants regard as their
invention; and*
*(B)   the claims must particularly point out and **distinctly define the metes and
bounds of the subject matter that will be protected by the patent grant**.*
*The first requirement is a subjective one because it is dependent on what the
applicants for a patent regard as their invention. The second requirement is an objective
one because it is not dependent on the views of applicant or any particular individual, but
is evaluated in the context of whether the claim is definite — i.e., whether the scope of the
claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent
art.*

Independent claims 1, 6, and 11 further recite limitations relating to "determining

an output of the node" in simulation based on the first, second and third state, which

makes it impossible for one skilled in the art to establish the metes and bounds of the

claim. The reference to "an output of the node" fails to point out specifically what is

included or **excluded** by the language of the claims, and it would be unclear to a

skilled artisan specifically how the first, second and third states are used to "determine"

the "output of the node". Independent claim 16 recites limitations relating to "storing

only three bits of state information", and then subsequently "checking the three bits in

simulating operation of the logic design". In this case, it is unclear specifically how the

bits are checked and what they are checked for in simulating the operation of the logic

design.

Dependent claims 2-5, 7-10, 12-15, and 17-21 inherit the defect of the claims

from which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.   Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent 6,044,211 issued to Jain in view of U.S. Patent 5,734,581 issued to

Butts et al.

<u>Independent claims 1, 6 and 11 are drawn to</u>:

Method, article, and apparatus for simulating a logic design by:
storing first state to identify node in simulation with logic high value;
storing second state to identify node in simulation with logic low value;
storing third state to identify node in simulation with undefined state;
determining output of node in simulation based on first state, second state, and third
state.

<u>Regarding independent claims 1, 6, and 11</u>: Jain discloses the simulation of a

logic design (Figs. 4-6) inclusive of identifying and storing the state(s) of the node

(CL13-L16-21, CL24-L17-26) and determining the output of the node (CL5-L55-59,

CL24-L29) during simulation based on value(s) of the prior state(s) (CL21-L29-33, 50,

61-63).

Jain does not explicitly disclose three distinct state values (i.e. high, low, and

undefined).

Butts specifically teaches multi-state realization of a logic design simulation using

three distinct logic states including high, low, and undefined (ambiguous). (Section 3.1.4

(all), CL67-L27-67, Fig. 50a-c) The examiner notes that these multi-state logic values

are also defined for use in logic design simulation by IEEE Standard 11-64-1993 for

VHDL models. (See: "IEEE Standard Multivalue Logic System for VHDL Model

Onteroperability", IEEE Standards Board, March 1993, pp. 2, 15-16)

It would have been obvious to one having ordinary skill in the art at the time the

claimed invention was made to modify the teachings of Jain relating to simulation of a

logic design and identifying and storing node state values, with the teachings of Butts

relating to the use of multi-state values in logic design simulation, to realize the claimed

invention. An obvious motivation exists since, in this case, the Jain reference teaches

to the Butts reference, and the Butts reference teaches to the Jain reference.

Specifically, both Jain and Butts teach simulation of a logic designs and are used in the

same technical arena as noted above. Jain teaches to Butts because Jain discloses that

node values can be detected and stored for a given state. (See: Jain, CL13-L16-21).

Butts teaches to Jain because Butts specifically discloses using multi-state values in

logic design simulation. (See: Butts, Section 3.1.4) Further, the level of skill required by

an artisan to realize the claimed limitations of the present invention is clearly

established by both references. (See: Jain/Butts, Abstracts) Accordingly, a skilled

artisan having access to the teachings of Jain and Butts, would have knowingly

modified the teachings of Jain with the teachings of Butts (or visa versa) to realize the

claimed elements of the present invention.

Per dependent claims 2, 7, and 12: Jain discloses determining node value based

on value(s) of prior state(s) (CL21-L29-33, 50, 61-63), Butts discloses determining a

high impedance state (CL67-L36) and hence would have been knowingly incorporated

using the reasoning cited above.

Per dependent claims 3, 8, and 13: This limitation would obviously be required

out of necessity since the third state represents an undefined state. That is, if two

sources are driving the node, then obviously the state of the node is undefined since the

value at the node will be somewhere in between the value of the first driving source,

and second driving source. (i.e. the output of the node is therefore ambiguous)

Per dependent claims 4, 9, and 14: Butts discloses a fourth state (high

impedance) in the logic design simulation (CL67-L36) and would have knowingly been

incorporated using the reasoning previously cited above.

Per dependent claims 5, 10, and 15: Jain discloses determining the node output

values based on selected values (high/low) of previous states as noted above. (CL5-

L35-63)

6.   Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable

over U.S. Patent 6,466,898 issued to Chan in view of U.S. Patent 6,738,875 issued

to Wang.

Per independent claim 22: Chan teaches a cycle-based simulation (CL1-L45-57,

CL2-L5-21, Figs. 3, 8, 11) of a logic design inclusive of logic computation instructions

(CL4-L5-19, Tab. 1) and multiple memory pages (CL8-L13-24).

Chan does not explicitly disclose a write-protected memory.

Wang teaches techniques for write protecting a memory page, copying to

secondary pages, un-protecting a write-protected page, rewriting values, and re-

protecting the original write protected page. (CL1-L55-CL2-L7, Figs. 5-7)

It would have been obvious to one having ordinary skill in the art at the time the

claimed invention was made to modify the teachings of Chan relating to a cycle-based

simulation, with the teachings of Wang relating to write protecting memory pages, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many cycle-based simulation tools available in the market place and large amounts of money being spent in product development and improvement. (See: Wang, Table 1, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have knowingly modified the teachings of Chan with the teachings of Wang in order to reduce development time and cost.

Per dependent claims 23-24: These claims merely require inserting an illegal instruction into the memory page to trigger an exception to the write protection process. This technique is well known in the art and would have knowingly been used by a skilled artisan as a method of generating a processor interrupt for handling write protection routine. (See: definition for "exception", Microsoft Computer Dictionary", Third Edition, 1997)

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   **Claims 16-17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 4,587,625 issued to Marino et al.**

Per independent claim 16: This claim merely requires storing three bits of state information, and then subsequently checking the three bits in simulating operation of the logic design. Marino discloses (CL2-L19-21) a three-bit method used in simulating logic for storing state/node information and then subsequently checking the logic value (high, low, etc.) of the three bits (CL10-L6-7).

Per dependent claims 17-19, and 21: Marino discloses determining the stored state/node value (high, low, etc.) based on three bits (CL2-L19-29, CL6-L2-10) and considers undermined states (CL11-32) and high impedance states (High "Z", Tab. IV).

Per dependent claim 20: Marino further discloses four-bit wide implementation of the state/node value storage technique cited above. (CL6-L17-19)

Conclusion

8.   *The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.*

U.S. Patent 6,718,522 issued to Mc Bride et al teaches simulating logic design and storing node state values.

"Process-Level Modeling with VHDL", J. Armstrong, Proceeding Verilog HDL Conference, March 1998, IEEE

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry

of a general nature relating to the status of this application should be directed to the

group receptionist whose telephone number is 571-272-3700. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can

be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
January 4, 2005